IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Patent Application of:	)	
Hisato **SHINOHARA** et al.	)	Confirmation No.: 2677
Application No.: 08/169,127	)	Examiner: Marianne L. Padgett
Filed: December 20, 1993	)	Art Unit: 1792
For: LASER IRRADIATION METHOD (AS AMENDED)	)	

MAIL STOP APPEAL BRIEF – PATENTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

APPEAL BRIEF (FOURTHLY-AMENDED)

This Appeal Brief is submitted in support of the Notice of Appeal filed May 16, 2007, and in further response to Notification of Non-Compliant Appeal Brief mailed October 16, 2008.

This Appeal responds to the November 17, 2006, final rejection of claims 61-80, 91-94, 101, 104-107, 131, and 140-180. Appellants respectfully request that the Board of Patent Appeals and Interferences reverse the final rejection of these claims.

If any additional fees are required or if the enclosed payment is insufficient, Appellant requests that the required fees be charged to Deposit Account No. 19-2380.

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I. REAL PARTY IN INTEREST

Semiconductor Energy Laboratory Co., Ltd., is the assignee and real party in interest.

II. RELATED APPEALS AND INTERFERENCES

At present, there are no related appeals or interferences known to the Appellants, the Appellants' representative or the assignee, which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

III. STATUS OF CLAIMS

Claims 1-60, 81-90, 95-100, 102-103, 108-130 & 132-139 have been canceled.

Claims 61-80, 91-94, 101, 104-107, 131, and 140-180 stand finally rejected and are the subject of this Appeal.

IV. STATUS OF AMENDMENTS

No amendment has been filed or submitted after the Final Office Action mailed November 17, 2006.

V. SUMMARY OF CLAIMED SUBJECT MATTER

This Appeal is taken from claims 61-80, 91-94, 101, 104-107, 131, and 140-180, of which claims 61, 66, 71, 76, 140, 141, 151, 152, 153, 154, 164, and 165 are independent.

The present invention relates to a method of manufacturing an active matrix display having active matrix circuit and a driving circuit for driving a liquid crystal device, disclosed, for example, on page 12, lines 22-23 of the present specification and in the descriptions of Figs. 1, 2A-2D, and 7A-7D. The method includes forming an ion blocking film 51 over a substrate 1, forming a semiconductor layer 52 comprising amorphous silicon over the ion blocking film 51. The method further including treating the active matrix with a laser 21 with a controlled beam shape, as shown in, e.g., Figs. 1, 2B, 2C and 2D, including the steps of providing a laser beam 21 having a first cross section, expanding 15 (Fig. 1), 22 (Fig. 1

and 2B) the first cross section in a first direction, condensing 16 (Fig. 1), 23 (Fig. 1 and 2C) the expanded laser beam in a second direction orthogonal to the first direction, irradiating the semiconductor layer 52 with the condensed laser beam 24 having a second cross section at a surface of the semiconductor layer 52 wherein a length of the second cross section in the first direction is longer than that of the first cross section and a width of the second cross section in the second direction is smaller than that of the first cross section, moving the substrate 1 along a third direction orthogonal to the first direction so that the semiconductor layer 52 is scanned with the condensed laser beam 24 to crystallize the semiconductor layer 52, and forming a plurality of TFTs using the crystallized semiconductor layer as at least channel regions of the TFTs.

The foregoing features are broadly encompassed in each of Appellant's independent claims 61, 66, 71, 76, 140, 141, 151, 152, 153, 154, 164, and 165 as follows:

Independent Claim 61

Independent claim 61 relates to a method of manufacturing an active matrix display device having an active matrix circuit and a driving circuit, wherein the method comprises forming an ion blocking film 51 over a substrate 1[1]; forming a non-single crystalline semiconductor layer 52[2]; providing a first laser beam 21 having a first cross section[3]; expanding 15 (Fig. 1), 22 (Fig. 1 and 2B) said first cross section of the first pulsed laser beam along a first direction[4]; condensing 16 (Fig. 1), 23 (Fig. 1 and 2C) the expanded laser beam along a second direction orthogonal to said first direction[5]; irradiating the non-single crystalline semiconductor layer 52 with the condensed laser beam 24 having a second cross section at a surface of the non-single crystalline semiconductor layer wherein a length of said

[1] See amendment to the specification (filed November 1, 2002) at page 10, fourth full paragraph continuing onto page 11, line 3, and Fig. 7A.

[2] See amendment to the specification (filed November 1, 2002) at page 10, fourth full paragraph continuing onto page 11, line 1, and Fig. 7A.

[3] See page 6, lines 4 and 20-22 of the specification and Fig. 1.

[4] See page 6, line 20-page 7, line 2 of the specification.

[5] See page 6, line 25-page 7, line 4 of the specification.

second cross section along said first direction is longer than that of said first cross section and a width of said second cross section along said second direction is smaller than that of said first cross section[6]; moving a relative location of said substrate 1 to the condensed laser beam 24 along a third direction orthogonal to said first direction while irradiating the non-single crystalline semiconductor layer 52 with the condensed laser beam 24 whereby the non-single crystalline semiconductor layer 52 is crystallized[7]; removing an insulating layer 59 comprising silicon oxide from an upper surface of the crystallized semiconductor layer[8]; and forming a plurality of thin film transistors using the crystallized semiconductor layer as at least channel regions of the thin film transistors for the active matrix circuit and said driving circuit[9].

Independent Claim 66

Independent claim 66 relates to a method of manufacturing an active matrix display device having an active matrix circuit and a driving circuit, wherein the method comprises forming an ion blocking film 51 over a substrate[10]; forming a non-single crystalline semiconductor layer 52 over said ion blocking film 51[11], said non-single crystalline semiconductor layer 52 being substantially intrinsic and doped with a dopant selected from the group consisting of boron and arsenic[12]; providing a first laser beam 21 having a first cross section[13]; expanding 15 (Fig. 1), 22 (Fig. 1 and 2B) said first cross section of the first pulsed laser beam along a first direction[14]; condensing 16 (Fig. 1), 23 (Fig. 1 and 2C) the

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[6] See page 6, line 20-page 7, lines 15 and page 8, lines 14-24 of the specification.

[7] See page 11, lines 12-27 of the specification and Fig. 8.

[8] See page 12, lines 1-4 of the specification and Figs. 7B and 7C.

[9] See page 12, lines 12-23 of the specification and Fig. 7C.

[10] See amendment to the specification (filed November 1, 2002) at page 10, fourth full paragraph continuing onto page 11, line 3, and Fig. 7A.

[11] See amendment to the specification (filed November 1, 2002) at page 10, fourth full paragraph continuing onto page 11, line 1, and Fig. 7A.

[12] See amendment to the specification (filed November 1, 2002) at page 10, fourth full paragraph continuing onto page 11, lines 4-6.

[13] See page 6, lines 4 and 20-22 of the specification and Fig. 1.

[14] See page 6, line 20-page 7, line 2 of the specification.

expanded laser beam along a second direction orthogonal to said first direction[15]; irradiating the non-single crystalline semiconductor layer 52 with the condensed laser beam 24 having a second cross section at a surface of the non-single crystalline semiconductor layer wherein a length of said second cross section along said first direction is longer than that of said first cross section and a width of said second cross section along said second direction is smaller than that of said first cross section[16]; moving a relative location of said substrate 1 to the condensed laser beam 24 along a third direction orthogonal to said first direction while irradiating the non-single crystalline semiconductor layer 52 with the condensed laser beam 24 whereby the non-single crystalline semiconductor layer 52 is crystallized[17]; and forming a plurality of thin film transistors using the crystallized semiconductor layer as at least channel regions of the thin film transistors for the active matrix circuit and said driving circuit[18].

Independent Claim 71

Independent claim 71 relates to a method of manufacturing an active matrix display device having an active matrix circuit and a peripheral circuit for driving pixel TFTs, wherein the method comprises forming an ion blocking film 51 over a substrate 1[19]; forming a non-single crystalline semiconductor layer 52 over said ion blocking film 51[20]; providing a first laser beam 21 having a first cross section[21]; expanding 15 (Fig. 1), 22 (Fig. 1 and 2B) said first cross section of the first pulsed laser beam along a first direction[22]; condensing 16 (Fig. 1), 23 (Fig. 1 and 2C) the expanded laser beam along a second direction orthogonal to said

[15] See page 6, line 25-page 7, line 4 of the specification.

[16] See page 6, line 20-page 7, lines 15 and page 8, lines 14-24 of the specification.

[17] See page 11, lines 12-27 of the specification and Fig. 8.

[18] See page 12, lines 12-23 of the specification and Fig. 7C.

[19] See amendment to the specification (filed November 1, 2002) at page 10, fourth full paragraph continuing onto page 11, line 3, and Fig. 7A.

[20] See amendment to the specification (filed November 1, 2002) at page 10, fourth full paragraph continuing onto page 11, line 1, and Fig. 7A.

[21] See page 6, lines 4 and 20-22 of the specification and Fig. 1.

[22] See page 6, line 20-page 7, line 2 of the specification.

first direction[23]; irradiating the non-single crystalline semiconductor layer 52 with the condensed laser beam 24 having a second cross section at a surface of the non-single crystalline semiconductor layer 52 wherein a length of said second cross section along said first direction is longer than that of said first cross section and a width of said second cross section along said second direction is smaller than that of said first cross section[24]; moving a relative location of said substrate 1 to the condensed laser beam 24 along a third direction orthogonal to said first direction while irradiating the non-single crystalline semiconductor layer 52 with the condensed laser beam 24 whereby the non-single crystalline semiconductor layer 52 is crystallized[25]; removing an insulating layer 59 comprising silicon oxide from an upper surface of the crystallized semiconductor layer[26]; and forming a plurality of thin film transistors using the crystallized semiconductor layer as at least channel regions of the thin film transistors for the active matrix circuit and said peripheral circuit[27].

Independent Claim 76

Independent claim 76 relates to a method of manufacturing an active matrix display device having an active matrix circuit and a peripheral circuit for driving pixel TFTs, wherein the method comprises forming an ion blocking film 51 over a substrate 1[28]; forming a non-single crystalline semiconductor layer 52 over said ion blocking 51, said non-single crystalline semiconductor layer 52 being substantially intrinsic and doped with a dopant selected from the group consisting of boron and arsenic[29]; providing a first laser beam 21 having a first cross section[30]; expanding 15 (Fig. 1), 22 (Fig. 1 and 2B)said first cross section

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[23] See page 6, line 25-page 7, line 4 of the specification.

[24] See page 6, line 20-page 7, line 15 and page 8, lines 14-24 of the specification.

[25] See page 11, lines 12-27 of the specification and Fig. 8.

[26] See page 12, lines 1-4 of the specification and Figs. 7B and 7C.

[27] See page 12, lines 12-23 of the specification and Fig. 7C.

[28] See amendment to the specification (filed November 1, 2002) at page 10, fourth full paragraph continuing onto page 11, line 3, and Fig. 7A.

[29] See amendment to the specification (filed November 1, 2002) at page 10, fourth full paragraph continuing onto page 11, lines 1 and 4-6, and Fig. 7A.

[30] See page 6, lines 4 and 20-22 of the specification and Fig. 1.

of the first pulsed laser beam a first direction[31]; condensing 16 (Fig. 1), 23 (Fig. 1 and 2C) the expanded laser beam along a second direction orthogonal to said first direction[32]; irradiating the non-single crystalline semiconductor layer 52 with the condensed laser beam 24 having a second cross section at a surface of the semiconductor layer wherein a length of said second cross section along said first direction is longer than that of said first cross section and a width of said second cross section along said second direction is smaller than that of said first cross section[33]; moving a relative location of said substrate 1 to the condensed laser beam 24 along a third direction orthogonal to said first direction so that the semiconductor layer is scanned with the condensed laser beam and whereby the semiconductor layer is crystallized[34]; and forming a plurality of thin film transistors using the crystallized semiconductor layer as at least channel regions of the thin film transistors for said active matrix circuit and said peripheral circuit[35].

Independent Claim 140

Independent claim 140 relates to a method of manufacturing an active matrix display device having an active matrix circuit and a driving circuit, wherein the method comprises forming an ion blocking film 51over a substrate 1[36]; forming a plurality of semiconductor islands 58 for said active matrix circuit and said driving circuit over the ion blocking film 51, each of said semiconductor islands comprising crystallized silicon[37]; forming a gate insulating film 53 on said plurality of semiconductor islands 58 wherein said gate insulating film 53 covers a surface of the ion blocking film 51[38], said surface being exposed between the

[31] See page 6, line 20-page 7, line 2 of the specification.

[32] See page 6, line 25-page 7, line 4 of the specification.

[33] See page 6, line 20-page 7, lines 15 and page 8, lines 14-24 of the specification.

[34] See page 11, lines 12-27 of the specification and Fig. 8.

[35] See page 12, lines 12-23 of the specification and Fig. 7C.

[36] See amendment to the specification (filed November 1, 2002) at page 10, fourth full paragraph continuing onto page 11, line 3, and Fig. 7A.

[37] See amendment to the specification (filed November 1, 2002) at page 10, fourth full paragraph continuing onto page 11, lines 8-9; page 11, lines 3-27 of the originally filed specification, Fig. 7B and 8.

[38] See page 12, lines 1-5 of the specification and Fig 7C.

plurality of semiconductor islands 58[39]; forming gate electrodes 56 over the semiconductor islands 58 with the gate insulating film 53 interposed therebetween[40], wherein the formation of said plurality of semiconductor islands 58 comprises steps of: providing a first laser beam 21 having a first cross section[41]; expanding 15 (Fig. 1), 22 (Fig. 1 and 2B) said first cross section of the first pulsed laser beam along a first direction[42]; condensing 16 (Fig. 1), 23 (Fig. 1 and 2C) the expanded laser beam along a second direction orthogonal to said first direction[43]; and directing the condensed laser beam 24 to the substrate 1 while moving a relative location of the substrate 1 to the condensed laser beam 24 along a third direction orthogonal to said first direction, wherein the condensed laser beam has a second cross section on the substrate wherein a length of said second cross section along said first direction is longer than that of said first cross section and a width of said second cross section along said second direction is smaller than that of said first cross section[44].

Independent Claim 141

Independent claim 141 relates to a method of manufacturing an active matrix display device having an active matrix circuit and a driving circuit, wherein the method comprises forming an ion blocking film 51 over a substrate 1[45]; forming a plurality of semiconductor islands 58 for said active matrix circuit and said driving circuit over the ion blocking film 51, each of said semiconductor islands 58 comprising crystallized silicon[46]; forming a gate insulating film 53 on said plurality of semiconductor islands 58[47]; forming metal gate electrodes 56 over the semiconductor islands 58 with the gate insulating film 53 interposed

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[39] See Fig. 7C

[40] See page 12, lines 5-11 of the specification and Fig 7C.

[41] See page 6, lines 4 and 20-22 of the specification and Fig. 1.

[42] See page 6, line 20-page 7, line 2 of the specification.

[43] See page 6, line 25-page 7, line 4 of the specification.

[44] See page 6, line 20-page 7, line 15; page 8, lines 14-24; page 11, lines 12-27 of the specification and Fig. 8.

[45] See amendment to the specification (filed November 1, 2002) at page 10, fourth full paragraph continuing onto page 11, line 3, and Fig. 7A.

[46] See amendment to the specification (filed November 1, 2002) at page 10, fourth full paragraph continuing onto page 11, lines 8-9; page 11, lines 3-27 of the originally filed specification, Fig. 7B and 8.

[47] See page 12, lines 1-5 of the specification and Fig 7C.

therebetween[48]; introducing an impurity into portions of the semiconductor islands 58 to form source and drain regions 57 in each of the semiconductor islands 58 with said gate electrodes 56 used as a mask[49], wherein the formation of said plurality of semiconductor islands 58 comprises steps of: providing a first laser beam 21 having a first cross section[50]; expanding 15 (Fig. 1), 22 (Fig. 1 and 2B) said first cross section of the first pulsed laser beam along a first direction[51]; condensing 16 (Fig. 1), 23 (Fig. 1 and 2C) the expanded laser beam along a second direction orthogonal to said first direction[52]; and directing the condensed laser beam 24 to the substrate 1 while moving a relative location of the substrate 1 to the condensed laser beam 24 along a third direction orthogonal to said first direction, wherein the condensed laser beam has a second cross section on the substrate wherein a length of said second cross section along said first direction is longer than that of said first cross section and a width of said second cross section along said second direction is smaller than that of said first cross section[53].

Independent Claim 151

Independent claim 151 relates to a method of manufacturing a plurality of thin film transistors, comprising the steps of forming an ion blocking film 51 over a substrate 1[54]; forming a non-single crystalline semiconductor layer 52 over said ion blocking film 51[55]; providing a first laser beam 21 having a first cross section[56]; expanding 15 (Fig. 1), 22 (Fig.

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[48] See page 12, lines 5-11; page 13, lines 5-7 of the specification and Fig 7C.

[49] See page 12, lines 8-11of the specification and Fig 7C.

[50] See page 6, lines 4 and 20-22 of the specification and Fig. 1.

[51] See page 6, line 20-page 7, line 2 of the specification.

[52] See page 6, line 25-page 7, line 4 of the specification.

[53] See page 6, line 20-page 7, line 15; page 8, lines 14-24; page 11, lines 12-27 of the specification and Fig. 8.

[54] See amendment to the specification (filed November 1, 2002) at page 10, fourth full paragraph continuing onto page 11, line 3, and Fig. 7A.

[55] See amendment to the specification (filed November 1, 2002) at page 10, fourth full paragraph continuing onto page 11, line 1, and Fig. 7A.

[56] See page 6, lines 4 and 20-22 of the specification and Fig. 1.

1 and 2B) said first cross section of the first pulsed laser beam along a first direction[57]; condensing 16 (Fig. 1), 23 (Fig. 1 and 2C) the expanded laser beam along a second direction orthogonal to said first direction[58]; irradiating the non-single crystalline semiconductor layer 52 with the condensed laser beam 24 having a second cross section at a surface of the non-single crystalline semiconductor layer wherein a length of said second cross section along said first direction is longer than that of said first cross section and a width of said second cross section along said second direction is smaller than that of said first cross section[59]; moving a relative location of said substrate 1 to the condensed laser beam 24 along a third direction orthogonal to said first direction while irradiating the non-single crystalline semiconductor layer 52 with the condensed laser beam 24 whereby the non-single crystalline semiconductor layer 52 is crystallized[60]; removing an insulating layer 59 comprising silicon oxide from an upper surface of the crystallized semiconductor layer[61]; and forming a plurality of thin film transistors using the crystallized semiconductor layer as at least channel regions of the thin film transistors[62].

Independent Claim 152

Independent claim 152 relates to a method of manufacturing a plurality of thin film transistors, comprising the steps of forming an ion blocking film 51 over a substrate 1[63]; forming a non-single crystalline semiconductor layer 52 over said ion blocking film 51[64], said non-single crystalline semiconductor layer 52 being substantially intrinsic and doped with a

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[57] See page 6, line 20-page 7, line 2 of the specification.

[58] See page 6, line 25-page 7, line 4 of the specification.

[59] See page 6, line 20-page 7, line 15 and page 8, lines 14-24 of the specification.

[60] See page 11, lines 12-27 of the specification and Fig. 8.

[61] See page 12, lines 1-4 of the specification and Figs. 7B and 7C.

[62] See page 12, lines 12-23 of the specification and Fig. 7C.

[63] See amendment to the specification (filed November 1, 2002) at page 10, fourth full paragraph continuing onto page 11, line 3, and Fig. 7A.

[64] See amendment to the specification (filed November 1, 2002) at page 10, fourth full paragraph continuing onto page 11, line 1, and Fig. 7A.

dopant selected from the group consisting of boron and arsenic[65]; providing a first laser beam 21 having a first cross section[66]; expanding 15 (Fig. 1), 22 (Fig. 1 and 2B) said first cross section of the first pulsed laser beam along a first direction[67]; condensing 16 (Fig. 1), 23 (Fig. 1 and 2C) the expanded laser beam along a second direction orthogonal to said first direction[68]; irradiating the non-single crystalline semiconductor layer 52 with the condensed laser beam 24 having a second cross section at a surface of the non-single crystalline semiconductor layer wherein a length of said second cross section along said first direction is longer than that of said first cross section and a width of said second cross section along said second direction is smaller than that of said first cross section[69]; moving a relative location of said substrate 1 to the condensed laser beam 24 along a third direction orthogonal to said first direction while irradiating the non-single crystalline semiconductor layer 52 with the condensed laser beam 24 whereby the non-single crystalline semiconductor layer 52 is crystallized[70]; and forming a plurality of thin film transistors using the crystallized semiconductor layer as at least channel regions of the thin film transistors[71].

Independent Claim 153

Independent claim 153 relates to a method of manufacturing a plurality of thin film transistors comprising: forming an ion blocking film 51 over a substrate 1[72]; forming a plurality of semiconductor islands 58 over the ion blocking film 51, each of said semiconductor islands 58 comprising crystallized silicon[73]; forming a gate insulating film 53

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[65] See amendment to the specification (filed November 1, 2002) at page 10, fourth full paragraph continuing onto page 11, lines 1 and 4-6, and Fig. 7A.

[66] See page 6, lines 4 and 20-22 of the specification and Fig. 1.

[67] See page 6, line 20-page 7, line 2 of the specification.

[68] See page 6, line 25-page 7, line 4 of the specification.

[69] See page 6, line 20-page 7, line 15 and page 8, lines 14-24 of the specification.

[70] See page 11, lines 12-27 of the specification and Fig. 8.

[71] See page 12, lines 12-23 of the specification and Fig. 7C.

[72] See amendment to the specification (filed November 1, 2002) at page 10, fourth full paragraph continuing onto page 11, line 3, and Fig. 7A.

[73] See amendment to the specification (filed November 1, 2002) at page 10, fourth full paragraph continuing onto page 11, lines 8-9; page 11, lines 3-27 of the originally filed specification, Fig. 7B and 8.

on said plurality of semiconductor islands 58 wherein said gate insulating film 53 covers a surface of the ion blocking film 51[74], said surface being exposed between the plurality of semiconductor islands 58[75]; forming gate electrodes 56 over the semiconductor islands 58 with the gate insulating film 53 interposed therebetween[76], wherein the formation of said plurality of semiconductor islands 58 comprises steps of: providing a first laser beam 21 having a first cross section[77]; expanding 15 (Fig. 1), 22 (Fig. 1 and 2B) said first cross section of the first pulsed laser beam along a first direction[78]; condensing 16 (Fig. 1), 23 (Fig. 1 and 2C) the expanded laser beam along a second direction orthogonal to said first direction[79]; and directing the condensed laser beam 24 to the substrate 1 while moving the substrate 1 along a third direction orthogonal to said first direction, wherein the condensed laser beam 24 has a second cross section on the substrate 1 wherein a length of said second cross section along said first direction is longer than that of said first cross section and a width of said second cross section along said second direction is smaller than that of said first cross section[80].

Independent Claim 154

Independent claim 154 relates to a method of manufacturing a plurality of thin film transistors comprising: forming an ion blocking film 51 over a substrate 1[81]; forming a plurality of semiconductor islands 58 over the ion blocking film 51, each of said semiconductor islands 58 comprising crystallized silicon[82]; forming a gate insulating film 53

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[74] See page 12, lines 1-5 of the specification and Fig 7C.

[75] See Fig. 7C

[76] See page 12, lines 5-11; page 13, lines 5-7 of the specification and Fig 7C.

[77] See page 6, lines 4 and 20-22 of the specification and Fig. 1.

[78] See page 6, line 20-page 7, line 2 of the specification.

[79] See page 6, line 25-page 7, line 4 of the specification.

[80] See page 6, line 20-page 7, line 15; page 8, lines 14-24; page 11, lines 12-27 of the specification and Fig. 8.

[81] See amendment to the specification (filed November 1, 2002) at page 10, fourth full paragraph continuing onto page 11, line 3, and Fig. 7A.

[82] See amendment to the specification (filed November 1, 2002) at page 10, fourth full paragraph continuing onto page 11, lines 8-9; page 11, lines 3-27 of the originally filed specification, Fig. 7B and 8.

on said plurality of semiconductor islands 58[83]; forming metal gate electrodes 56 over the semiconductor islands 58 with the gate insulating film 53 interposed therebetween[84]; introducing an impurity into portions of the semiconductor islands 58 to form source and drain regions 57 in each of the semiconductor islands 58 with said gate electrodes 56 used as a mask[85], wherein the formation of said plurality of semiconductor islands 58 comprises steps of: providing a first laser beam 21 having a first cross section[86]; expanding 15 (Fig. 1), 22 (Fig. 1 and 2B) said first cross section of the first pulsed laser beam along a first direction[87]; condensing 16 (Fig. 1), 23 (Fig. 1 and 2C) the expanded laser beam along a second direction orthogonal to said first direction[88]; and directing the condensed laser beam 24 to the substrate 1 while moving the substrate 1 along a third direction orthogonal to said first direction, wherein the condensed laser beam 24 has a second cross section on the substrate 1 wherein a length of said second cross section along said first direction is longer than that of said first cross section and a width of said second cross section along said second direction is smaller than that of said first cross section[89].

Independent Claim 164

Independent claim 164 relates to a method of manufacturing an active matrix display device having an active matrix circuit and a peripheral circuit for driving pixel TFTs, wherein the method comprises forming an ion blocking film 51 over a substrate 1[90]; forming a plurality of semiconductor islands 58 for said active matrix circuit and said peripheral circuit over the ion blocking film 51, each of said semiconductor islands 58 comprising crystallized

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[83] See page 12, lines 1-5 of the specification and Fig 7C.

[84] See page 12, lines 5-11; page 13, lines 5-7 of the specification and Fig 7C.

[85] See page 12, lines 8-11of the specification and Fig 7C.

[86] See page 6, lines 4 and 20-22 of the specification and Fig. 1.

[87] See page 6, line 20-page 7, line 2 of the specification.

[88] See page 6, line 25-page 7, line 4 of the specification.

[89] See page 6, line 20-page 7, line 15; page 8, lines 14-24; page 11, lines 12-27 of the specification and Fig. 8.

[90] See amendment to the specification (filed November 1, 2002) at page 10, fourth full paragraph continuing onto page 11, line 3, and Fig. 7A.

silicon[91]; forming a gate insulating film 53 on said plurality of semiconductor islands 58 wherein said gate insulating film 53 covers a surface of the ion blocking film 51, said surface being exposed between the plurality of semiconductor islands 58[92]; forming gate electrodes 56 over the semiconductor islands 58 with the gate insulating film 53 interposed therebetween[93], wherein the formation of said plurality of semiconductor islands 58 comprises steps of: providing a first laser beam 21 having a first cross section[94]; expanding 15 (Fig. 1), 22 (Fig. 1 and 2B) said first cross section of the first pulsed laser beam along a first direction[95]; condensing 16 (Fig. 1), 23 (Fig. 1 and 2C) the expanded laser beam along a second direction orthogonal to said first direction[96]; and directing the condensed laser beam 24 to the substrate 1 while moving the substrate 1 along a third direction orthogonal to said first direction, wherein the condensed laser beam 24 has a second cross section on the substrate wherein a length of said second cross section along said first direction is longer than that of said first cross section and a width of said second cross section along said second direction is smaller than that of said first cross section[97].

Independent Claim 165

Independent claim 165 relates to a method of manufacturing an active matrix display device having an active matrix circuit and a peripheral circuit, wherein the method comprises forming an ion blocking film 51 over a substrate 1[98]; forming a plurality of semiconductor islands 58 for said active matrix circuit and said peripheral circuit over the ion blocking film

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[91] See amendment to the specification (filed November 1, 2002) at page 10, fourth full paragraph continuing onto page 11, lines 8-9; page 11, lines 3-27 of the originally filed specification, Fig. 7B and 8.

[92] See Fig. 7C

[93] See page 12, lines 5-11 of the specification and Fig 7C.

[94] See page 6, lines 4 and 20-22 of the specification and Fig. 1.

[95] See page 6, line 20-page 7, line 2 of the specification.

[96] See page 6, line 25-page 7, line 4 of the specification.

[97] See page 6, line 20-page 7, line 15; page 8, lines 14-24; page 11, lines 12-27 of the specification and Fig. 8.

[98] See amendment to the specification (filed November 1, 2002) at page 10, fourth full paragraph continuing onto page 11, line 3, and Fig. 7A.

51, each of said semiconductor islands 58 comprising crystallized silicon[99]; forming a gate insulating film 53 on said plurality of semiconductor islands 58; forming metal gate electrodes 56 over the semiconductor islands 58 with the gate insulating film 53 interposed therebetween[100]; introducing an impurity into portions of the semiconductor islands 58 to form source and drain regions 57 in each of the semiconductor islands 58 with said gate electrodes 56 used as a mask[101], wherein the formation of said plurality of semiconductor islands 58 comprises steps of: providing a first laser beam 21 having a first cross section[102]; expanding 15 (Fig. 1), 22 (Fig. 1 and 2B) said first cross section of the first pulsed laser beam along a first direction[103]; condensing 16 (Fig. 1), 23 (Fig. 1 and 2C) the expanded laser beam along a second direction orthogonal to said first direction[104]; and directing the condensed laser beam 24 to the substrate 1 while moving a relative location of the substrate 1 to the condensed laser beam 24 along a third direction orthogonal to said first direction, wherein the condensed laser beam 24 has a second cross section on the substrate wherein a length of said second cross section along said first direction is longer than that of said first cross section and a width of said second cross section along said second direction is smaller than that of said first cross section[105].

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[99] See amendment to the specification (filed November 1, 2002) at page 10, fourth full paragraph continuing onto page 11, lines 8-9; page 11, lines 3-27 of the originally filed specification, Fig. 7B and 8.

[100] See page 12, lines 5-11; page 13, lines 5-7 of the specification and Fig 7C.

[101] See page 12, lines 8-11of the specification and Fig 7C.

[102] See page 6, lines 4 and 20-22 of the specification and Fig. 1.

[103] See page 6, line 20-page 7, line 2 of the specification.

[104] See page 6, line 25-page 7, line 4 of the specification.

[105] See page 6, line 20-page 7, line 15; page 8, lines 14-24; page 11, lines 12-27 of the specification and Fig. 8.

VI. GROUND OF REJECTION TO BE REVIEWED ON APPEAL

The grounds of rejection to be reviewed on appeal are as follows:

Claims 61-65, 71-75, 91, 144, 151, 155-163, 166-167 and 173-175 stand rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 61-65, 71-75, 91, 144, 151, 155-163, 166-167, 173-175, and 176-180 stand rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement.

Claims 61-65, and 71-75 stand rejected under 35 U.S.C. § 112, first paragraph, for allegedly not enabling any person skilled in the art to which it pertains, or with which it is most nearly connected, to use the invention commensurate in scope with these claims.

Claims 71-80, 93-94, 101, and 106-107 stand objected to because of informalities.

Claims 61-80, 91-94, 101, 104-107, 131, and 140-175 stand rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-39 of U.S. Patent No. 6,261,856 B1 to Shinohara et al.

VII. ARGUMENTS

The Rejection Under 35 U.S.C. § 112, second paragraph should be Reversed

Claims 61-65, 71-75, 91, 144, 151, 155-163, 166-167 and 173-175 stand rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Appellants appeal this rejection and request reversal for at least the reasons set forth hereinbelow.

Specifically, the Examiner states that the feature of "removing an insulating layer comprising silicon oxide from an upper surface of the crystallized semiconductor layer" is

unclear. Moreover, the Examiner questions "where this silicon oxide layer comes from, since it was never claim(ed) to be deposited, hence it is unclear how [caught] one can remove something that does not necessarily exist" (see e.g., Final Office Action, mailed on November 17, 2006, at page 2, lines 6-9).

Generally, the standard under 35 U.S.C. § 112, second paragraph, is whether the claims, when read in light of the specification, reasonably apprize those skilled in art of the scope of the claimed invention. See, e.g., *Miles Labs., Inc. v. Shandon*, 997 F.2d 870, 875 (Fed. Cir. 1993). The Manual of Patent Examining Procedure ("MPEP") specifically provides that the breadth or scope of protection afforded by the claimed terminology is not to be equated with indefiniteness. (See, e.g., M.P.E.P. § 2173.04.) If the scope of the subject matter embraced by the claims is clear, and if applicants have not otherwise indicated that they intend the invention to be of a scope different from that defined in the claims, then the claims comply with 45 U.S. C. 112, second paragraph.

Appellants respectfully submit that the feature including the removal of the insulating layer, as recited, for example, in independent claims 61, 71, and 151 are sufficiently supported by the specification, at least, on page 12, lines 1-4. The specification clearly conveys that an insulating layer 53 is formed on the substrate shown in Fig. 7(c). The insulating layer 53 is disclosed to be formed by sputtering. By way of example, one embodiment of the insulating layer 53 is disclosed to be made of silicon oxide. Thus, the question, as proposed by the Examiner, as to "where this silicon oxide layer comes from" is clearly addressed within Appellants specification. Furthermore, in accordance with the requirements of the MPEP, those skilled in the art would be reasonably apprized as to the scope of the claimed invention since one of ordinary skill in the art would readily appreciate the possible presence of an oxide layer requiring removal. Thus, the specification clearly provides enablement for formation of an oxide layer. Furthermore, the scope of the claims include coverage of treating an oxide which is formed during laser irradiation.

The Examiner also states (e.g., page 2, lines 9-11 of the aforementioned Final Office) that "(i)t also leaves the claim open to speculation, such as since this insulating layer was not necessarily present when irradiation occurred, did they irradiation while crystallizing the

semiconductor layer, also cause surface oxidation?" However, in view of the Interview Summary of June 6, 2007, the Examiner states that "the inclusion of the limitations of claims 176-180 in their independent claims would correct the 112, second paragraph problem set forth in section 1 of the action mailed 11/17/2006." Specifically, the claims recite a feature including "said insulating layer comprising silicon oxide is formed before the irradiating with the condensed laser beam." Accordingly, claims 176-180 should be considered separately and removed from this rejection.

Further, each of the dependent claims depend from one of independent claims 61, 71, or 151 and also overcome the rejection under 35 U.S.C. § 112, second paragraph, for at least the same reasons as set forth above with respect to claims 61, 71, or 151.

The Rejection Under 35 U.S.C. § 112, first paragraph should be Reversed

Claims 61-65, 71-75, 91, 144, 151, 155-163, 166-167, 173-175, and 176-180 stand rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement. Appellants appeal this rejection and request reversal for at least the reasons set forth hereinbelow.

Specifically, the Examiner states that the "claim(s) contains subject matter, which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention . . . (a)s noted above, the scope of the claim is inclusive of options that are broader than the scope of the enabling disclosure. Also new claims 176-180 are lacking with respect to their relationship of where they reside during the crystallization, i.e., as an intervening layer between the irradiation source and the semiconductor layer. While the claims are inclusive of this option, they are not restricted [thereto] as exemplified above, hence [the claims] still encompass options not supported by the more specific disclosure of the specification." (See, section 2 of Final Office Action, mailed on November 17, 2006.)

This rejection is improper. The MPEP specifically states that claimed subject matter "need not be described literally (i.e., using the same terms or *in haec verba*) in order for the

disclosure to satisfy the description requirement." *Id.* As the Federal Circuit in *Cordis Corp. v. Medtronic AVE, Inc.*, 339 F.3d 1352 (Fed. Cir. 2003), explained:

> The disclosure as originally filed does **not**, however, have to provide in *haec verba* support for the claimed subject matter at issue.

Id. At 1364. And the MPEP also provides that the Examiner has the burden of demonstrating how the original disclosure, including the specification, claims and drawings, fail to describe the claimed subject matter in such a way as to reasonably convey to one skilled in the art that the inventor had possession of the clamed invention (e.g., see M.P.E.P. § 2163.02 (8th Ed. Rev. 5, August 2006)) since one of ordinary skill in the art would readily appreciate the possible presence of an oxide layer requiring removal.

In this case, the Examiner has failed to meet this burden. Most notably, claims 176-180 are rejected only under 35 U.S.C. § 112, first paragraph. As argued during the Interview of June 6, 2007, the rejection is improper, because consideration has not been given to "the whole" of each of the claims. More specifically, each of claims 61, 71, 144, 151, and 168, from which dependent claims 176-180 respectively depend, specifically recite that the oxide is removed from "an upper surface of the crystallized layer." The combination of these features with features of forming the insulating layer comprising silicon oxide before crystallization is fully supported by an exemplary embodiment described in the specification. (See, for example, Appellants' specification at the last line of page 10 to the first line of page 12.) Furthermore, where the oxide layer resides during crystallization is implicit from claims 176-180 (i.e., "upper surface" of the semiconductor layer). It is further noted that the Examiner concludes in the aforementioned Interview that "claims 176-180 . . . would also appear to correct the first paragraph 112 problems set forth in section 2." Thus, withdrawal of the rejection is respectfully requested, particularly as the claims 176-180.

Claims 61-65, and 71-75 stand rejected under 35 U.S.C. § 112, first paragraph, for allegedly not enabling any person skilled in the art to which it pertains, or with which it is most nearly connected, to use the invention commensurate in scope with these claims. Appellants appeal this rejection and request reversal for at least the reasons set forth hereinbelow.

Specifically, the Examiner states that the "the specification . . .does not reasonably provide enablement for removal of 'an insulating layer comprising silicon oxide' from an unknown source in an uncertain relationship to the irradiation step itself." However, the specification does provide support for this claimed feature as outlined above. In addition, the Examiner agrees in the Interview of June 6, 2007, that "claims 176-180 . . . would also appear to correct the first paragraph 112 problems set forth in section 2" to which Appellants are amenable to incorporating into the independent claims.

The Objection of the Claims due to Informalities

Claims 71-80, 93-94, 101, and 106-107 stand objected to because of informalities. Appellants appeal this rejection and request reversal for at least the reasons set forth hereinbelow.

Specifically, the Examiner is requiring that acronyms and abbreviations employed in the claims should on first usage in a claim sequence, be written out in order to clearly define them. While it is believed that skilled artisans within the same field of endeavor would readily recognize and know the meaning of "TFT" to mean "thin film transistor", Appellants are amenable to editing the claims to include the terms "thin film transistor" as requested by the Examiner.

The Rejection Under the Judicially Created Doctrine of Obviousness-type Double Patenting should be Reversed

Claims 61-80, 91-94, 101, 104-107, 131, and 140-175 stand rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-39 of U.S. Patent No. 6,261,856 B1 to Shinohara et al. Appellants appeal this rejection and request reversal for at least the reasons set forth hereinbelow.

Of the rejected claims, claims 61, 66, 71, 76, 140, 141, 151, 152, 153, 154, 164, and 165 are independent. Shinohara et al. fails to render the claimed invention unpatentable.

Each of the claims recite a specific combination of features that distinguishes the invention from the prior art in different ways. For example, independent claims 61, 71, and 151 recite a combination that includes, among other things:

> *removing an insulating layer comprising silicon oxide from an upper surface of the crystallized semiconductor layer.*

The Examiner states in section 3 of the Final Office action that the aforementioned removing feature "cannot affect differentiation as it is unclear how to remove a layer which may not be present." However, as previously outlined above, the claim recitation is clear and properly supported by the MPEP and provides a clear distinction from the prior art.

Independent claims 66, 76, and 152 recite yet another combination that includes, inter alia,

> *moving a relative location of said substrate to the condensed laser beam along a third direction orthogonal to said first direction.*

While the Examiner contends that "these limitations added to the claims do not provide significant differentiation," Appellants respectfully assert that, indeed, these features are clearly different than that disclosed by Shinohara et al. Shinohara et al. discusses a method for treating an object with a laser including emitting a laser beam from a laser. As discussed in Appellants' specification (e.g., page 11, lines 26-27), either one of the laser optical system or substrate may be moved. Thus, a relative location of the substrate is moved to the condensed laser beam along a third direction orthogonal to the first direction as recited by at least claims 66, 76, and 152. Hence, the claims of Shinohara et al. fail to disclose or fairly suggest moving the relative location in the direction as claimed. Therefore, the rejection is improper and should be reversed accordingly.

Additionally, independent claims 140, 153, and 164 recite another combination that includes, for example,

> *forming a gate insulating film on said plurality of semiconductor islands wherein said gate insulating film covers a surface of the ion blocking film, said surface being exposed between the plurality of semiconductor islands.*

These features are not addressed by the claims of Shinohara et al. In the Interview Summary of June 6, 2007, the Examiner purports that the presence of specific ion blocking films do not specify either positively or negatively that the gate insulating films are covering the ion blocking film and further questions why the presence or the lack of the gate insulator over the ion blocking film makes a critical difference. The Examiner further asserts that such critical difference would need to be sufficiently shown to overcome the obviousness double patenting rejection. However, Appellants contend that support and criticality of the aforementioned features have already been expressed, for example, in descriptions of the filed specification and drawings. For example, turning to page 1, lines 13-22 and page 2, lines 9-23 of the specification, problems of well-known techniques for producing patterns in thin films formed on surfaces are described. Advantages produced by the present disclosure are described, for example, on page 3, lines 2-4. Additional key points for improving the configuration of the pattern begin on page 3 at line 9. Fig. 7C provides further support in demonstrating the criticality of the features recited claims 140, 153, and 164. Thus, the Examiner's concerns have been obviated by this showing in accordance with the MPEP. This rejection, therefore, cannot be sustained.

Furthermore, independent claims 71, 76, 164, and 165 recite yet another combination that includes, inter alia,

> *forming a plurality of thin film transistors . . . for the active matrix circuit and said peripheral circuit.*

The claims of Shinohara et al. do not disclose or fairly suggest the aforementioned features. The Examiner has not further provided or addressed why these features would have been obvious in view of Shinohara et al. Again, however, in the June 6, 2007 interview, the Examiner requests a showing of criticality for these features and questions the term "peripheral circuit". Appellants, again, maintain that criticality is, at least, demonstrated within the filed specification in addressing the problems of well-known techniques for producing patterns in thin films formed on surface as outlined above (e.g., see page 1, lines 13-22 and page 2, lines 9-23). Advantages of the present disclosure, resulting therefrom, are again described, for example, on page 3, lines 2-4. Support for the term "peripheral circuit" is also found, at least, in Appellant's Figs. 5A, 5B, and 8. Furthermore, support for forming

semiconductor islands of a substrate in order to form a driver circuit or peripheral circuit is found, at least, on page 11 lines 9-11. As explained during the aforementioned interview, the term "peripheral circuit" is a term of the art readily understood by skilled artisans within the same claimed environment. This is further evidenced, at least, by U.S. Patent Numbers 7,381,599 B2[106] and 7,416,907 B2[107] in which the term is utilized within the same field of endeavor. Thus, regarding the term "peripheral circuit", one of ordinary skill in the art would readily recognize this term of art. Further, the MPEP provides that the Examiner has the burden of demonstrating how the original disclosure, including the specification, claims and drawings, fail to describe the claimed subject matter in such a way as to reasonably convey to one skilled in the art that the inventor had possession of the clamed invention. (See M.P.E.P. § 2163.02 (8th Ed. Rev. 5, August 2006).) This rejection, therefore, cannot be sustained.

Moreover, independent claims 141 and 154 recite yet another combination that includes, inter alia,

> *wherein the condensed laser beam has a second cross section on the substrate wherein a length of said second cross section along said first direction is longer than that of said first cross section and a width of said second cross section along said second direction is smaller than that of said first cross section.*

While the claims of Shinohara et al. recite a wavelength of the laser beam (e.g., claim 2), the claims fail to anticipate or render obvious the features as recited by claims 141 and 154. This rejection, therefore, cannot be sustained.

At the very least, Shinohara et al. fails to disclose or suggest any of these exemplary features recited in the independent claims 61, 66, 71, 76, 140, 141, 151, 152, 153, 154, 164, and 165 for, at least, the reasons expressed herein. Accordingly, Appellants respectfully request the Board to reverse the final rejection of these claims.

In addition, each of the dependent claims also recite combinations that are separately patentable. Each of the dependent claims depend from one of independent claims 61, 66, 71,

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[106] See col. 6, line 50; col. 8, line 27; col. 10, line 18; and col. 14, line 37.

[107] See col. 5, line 64; col. 6, lines 5, 14, 34, 40, 43, 50, and 59; col. 14, line 64; and col. 16, line 66.

76, 140, 141, 151, 152, 153, 154, 164, or 165 and are patentable over the cited prior art for at least the same reasons as set forth above with respect to claims 61, 66, 71, 76, 140, 141, 151, 152, 153, 154, 164, and 165. Accordingly, Appellants also respectfully request the Board to reverse the final rejections of each of the dependent claims.

VIII. CONCLUSION

Since the Examiner's final rejections under 35 U.S.C. § 112, first and second paragraph, and the judicially created doctrine of obviousness-type double patenting are inappropriate for the reasons set forth above, Appellants respectfully request the Board to reverse each ground of the rejections.

Respectfully submitted,
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Date: November 17, 2008

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IX. CLAIMS APPENDIX

1-60. (Canceled)

61. A method of manufacturing an active matrix display device having an active matrix circuit and a driving circuit, said method comprising:

forming an ion blocking film over a substrate;

forming a non-single crystalline semiconductor layer;

providing a first laser beam having a first cross section;

expanding said first cross section of the first pulsed laser beam along a first direction;

condensing the expanded laser beam along a second direction orthogonal to said first direction;

irradiating the non-single crystalline semiconductor layer with the condensed laser beam having a second cross section at a surface of the non-single crystalline semiconductor layer wherein a length of said second cross section along said first direction is longer than that of said first cross section and a width of said second cross section along said second direction is smaller than that of said first cross section;

moving a relative location of said substrate to the condensed laser beam along a third direction orthogonal to said first direction while irradiating the non-single crystalline semiconductor layer with the condensed laser beam whereby the non-single crystalline semiconductor layer is crystallized;

removing an insulating layer comprising silicon oxide from an upper surface of the crystallized semiconductor layer; and

forming a plurality of thin film transistors using the crystallized semiconductor layer as at least channel regions of the thin film transistors for the active matrix circuit and said driving circuit.

62. The method according to claim 61 wherein said laser beam is an excimer laser beam.

63. The method according to claim 61 wherein said ion blocking film comprises silicon oxide.

64. The method according to claim 61 wherein said ion blocking film comprises silicon nitride.

65. The method according to claim 61 wherein said ion blocking film comprises non-doped silicon oxide.

66. A method of manufacturing an active matrix display device having an active matrix circuit and a driving circuit, said method comprising:

forming an ion blocking film over a substrate;

forming a non-single crystalline semiconductor layer over said ion blocking film, said non-single crystalline semiconductor layer being substantially intrinsic and doped with a dopant selected from the group consisting of boron and arsenic;

providing a first laser beam having a first cross section;

expanding said first cross section of the first pulsed laser beam along a first direction;

condensing the expanded laser beam along a second direction orthogonal to said first direction;

irradiating the non-single crystalline semiconductor layer with the condensed laser beam having a second cross section at a surface of the non-single crystalline semiconductor layer wherein a length of said second cross section along said first direction is longer than that of said first cross section and a width of said second cross section along said second direction is smaller than that of said first cross section;

moving a relative location of said substrate to the condensed laser beam along a third direction orthogonal to said first direction while irradiating the non-single crystalline semiconductor layer with the condensed laser beam whereby the non-single crystalline semiconductor layer is crystallized; and

forming a plurality of thin film transistors using the crystallized semiconductor layer as at least channel regions of the thin film transistors for the active matrix circuit and said driving circuit.

67. The method according to claim 66 wherein said laser beam is an excimer laser beam.

68. The method according to claim 66 wherein said ion blocking film comprises silicon oxide.

69. The method according to claim 66 wherein said ion blocking film comprises silicon nitride.

70. The method according to claim 66 wherein said ion blocking film comprises non-doped silicon oxide.

71. A method of manufacturing an active matrix display device having an active matrix circuit and a peripheral circuit for driving pixel TFTs, said method comprising:

forming an ion blocking film over a substrate;

forming a non-single crystalline semiconductor layer over said ion blocking film;

providing a first laser beam having a first cross section;

expanding said first cross section of the first pulsed laser beam along a first direction;

condensing the expanded laser beam along a second direction orthogonal to said first direction;

irradiating the non-single crystalline semiconductor layer with the condensed laser beam having a second cross section at a surface of the non-single crystalline semiconductor layer wherein a length of said second cross section along said first direction is longer than that of said first cross section and a width of said second cross section along said second direction is smaller than that of said first cross section;

moving a relative location of said substrate to the condensed laser beam along a third direction orthogonal to said first direction while irradiating the non-single crystalline semiconductor layer with the condensed laser beam whereby the non-single crystalline semiconductor layer is crystallized;

removing an insulating layer comprising silicon oxide from an upper surface of the crystallized semiconductor layer; and

forming a plurality of thin film transistors using the crystallized semiconductor layer as at least channel regions of the thin film transistors for the active matrix circuit and said peripheral circuit.

72. The method according to claim 71 wherein said laser beam is an excimer laser beam.

73. The method according to claim 71 therein said ion blocking film comprises silicon oxide.

74. The method according to claim 71 wherein said ion blocking film comprises silicon nitride.

75. The method according to claim 71 wherein said ion blocking film comprises non-doped silicon oxide.

76. A method of manufacturing an active matrix display device having an active matrix circuit and a peripheral circuit for driving pixel TFTs, said method comprising:

forming an ion blocking film over a substrate;

forming a non-single crystalline semiconductor layer over said ion blocking, said non-single crystalline semiconductor layer being substantially intrinsic and doped with a dopant selected from the group consisting of boron and arsenic;

providing a first laser beam having a first cross section;

expanding said first cross section of the first pulsed laser beam a first direction;

condensing the expanded laser beam along a second direction orthogonal to said first direction;

irradiating the non-single crystalline semiconductor layer with the condensed laser beam having a second cross section at a surface of the semiconductor layer wherein a length of said second cross section along said first direction is longer than that of said first cross section and a width of said second cross section along said second direction is smaller than that of said first cross section;

moving a relative location of said substrate to the condensed laser beam along a third direction orthogonal to said first direction so that the semiconductor layer is scanned with the condensed laser beam and whereby the semiconductor layer is crystallized; and

forming a plurality of thin film transistors using the crystallized semiconductor layer as at least channel regions of the thin film transistors for said active matrix circuit and said peripheral circuit.

77. The method according to claim 76 wherein said laser beam is an excimer laser beam.

78. The method according to claim 76 wherein said ion blocking film comprises silicon oxide.

79. The method according to claim 76 wherein said ion blocking film comprises silicon nitride.

80. The method according to claim 76 wherein said ion blocking film comprises non-doped silicon oxide.

81. -90. (Canceled)

91. The method according to claim 61 further comprising a step of removing a peripheral portion of the expanded laser beam through a mask before the step of condensing the expanded laser beam wherein said peripheral portion includes at least edges of the expanded laser beam extending along said first direction.

92. The method according to claim 66 further comprising a step of removing a peripheral portion of the expanded laser beam through a mask before the step of condensing the expanded laser beam wherein said peripheral portion includes at least edges of the expanded laser beam extending along said first direction.

93. The method according to claim 71 further comprising a step of removing a peripheral portion of the expanded laser beam through a mask before the step of condensing the expanded laser beam wherein said peripheral portion includes at least edges of the expanded laser beam extending along said first direction.

94. The method according to claim 76 further comprising a step of removing a peripheral portion of the expanded laser beam through a mask before the step of condensing the expanded laser beam wherein said peripheral portion includes at least edges of the expanded laser beam extending along said first direction.

95. -100. (Canceled)

101. The method according to claim 76 wherein said substrate is a soda-lime glass.

102. -103. (Canceled)

104. The method according to claim 61 wherein said active matrix display device is a liquid crystal device.

105. The method according to claim 66 wherein said active matrix display device is a liquid crystal device.

106. The method according to claim 71 wherein said active matrix display device is a liquid crystal device.

107. The method according to claim 76 wherein said active matrix display device is a liquid crystal device.

108 -130. (Canceled)

131. The method according to claim 61 wherein said laser beam is a pulsed laser

beam and said substrate is moved in a stepwise manner.

132. -139. (Canceled)

140. A method of manufacturing an active matrix display device having an active matrix circuit and a driving circuit, said method comprising:

forming an ion blocking film over a substrate;

forming a plurality of semiconductor islands for said active matrix circuit and said driving circuit over the ion blocking film, each of said semiconductor islands comprising crystallized silicon;

forming a gate insulating film on said plurality of semiconductor islands wherein said gate insulating film covers a surface of the ion blocking film, said surface being exposed between the plurality of semiconductor islands;

forming gate electrodes over the semiconductor islands with the gate insulating film interposed therebetween,

wherein the formation of said plurality of semiconductor islands comprises steps of:

providing a first laser beam having a first cross section;

expanding said first cross section of the first pulsed laser beam along a first direction;

condensing the expanded laser beam along a second direction orthogonal to said first direction; and

directing the condensed laser beam to the substrate while moving a relative location of the substrate to the condensed laser beam along a third direction orthogonal to said first direction,

wherein the condensed laser beam has a second cross section on the substrate wherein a length of said second cross section along said first direction is longer than that of said first cross section and a width of said second cross section along said second direction is smaller than that of said first cross section.

141. A method of manufacturing an active matrix display device having an active matrix circuit and a driving circuit, said method comprising:

forming an ion blocking film over a substrate;

forming a plurality of semiconductor islands for said active matrix circuit and said driving circuit over the ion blocking film, each of said semiconductor islands comprising crystallized silicon;

forming a gate insulating film on said plurality of semiconductor islands;

forming metal gate electrodes over the semiconductor islands with the gate insulating film interposed therebetween;

introducing an impurity into portions of the semiconductor islands to form source and drain regions in each of the semiconductor islands with said gate electrodes used as a mask,

wherein the formation of said plurality of semiconductor islands comprises steps of:

providing a first laser beam having a first cross section;

expanding said first cross section of the first pulsed laser beam along a first direction;

condensing the expanded laser beam along a second direction orthogonal to said first direction; and

directing the condensed laser beam to the substrate while moving a relative location of the substrate to the condensed laser beam along a third direction orthogonal to said first direction,

wherein the condensed laser beam has a second cross section on the substrate wherein a length of said second cross section along said first direction is longer than that of said first cross section and a width of said second cross section along said second direction is smaller than that of said first cross section.

142. The method according to claim 61 or 66 wherein said non-single crystalline semiconductor layer comprises amorphous silicon.

143. The method according to claim 61 or 66 wherein said non-single crystalline semiconductor layer comprises solid phase crystallized silicon.

144. The method according to claim 66 further comprising a step of removing an insulating layer comprising silicon oxide from an upper surface of the crystallized semiconductor layer.

145. The method according to any one of claim 140 to 141 wherein said ion blocking film comprises silicon oxide.

146. The method according to any one of claim 140 to 141 wherein said ion blocking film comprises silicon nitride.

147. The method according to any one of claim 140 to 141 wherein said ion blocking film comprises non-doped silicon oxide.

148. The method according to any one of claim 140 and 141 further comprising a step of removing a peripheral portion of the expanded laser beam through a mask before the step of condensing the expanded laser beam wherein said peripheral portion includes at least edges of the expanded laser beam extending along said first direction.

149. The method according to any one of claim 61, 66, 140 and 141 wherein said substrate is moved.

150. The method according to any one of claim 61, 66, 140 and 141 wherein said ion blocking film blocks sodium from the substrate.

151. A method of manufacturing a plurality of thin film transistors, comprising steps of:

forming an ion blocking film over a substrate;

forming a non-single crystalline semiconductor layer over said ion blocking film;

providing a first laser beam having a first cross section;

expanding said first cross section of the first pulsed laser beam along a first direction;

condensing the expanded laser beam along a second direction orthogonal to said first direction;

irradiating the non-single crystalline semiconductor layer with the condensed laser beam having a second cross section at a surface of the non-single crystalline semiconductor layer wherein a length of said second cross section along said first direction is longer than

that of said first cross section and a width of said second cross section along said second direction is smaller than that of said first cross section;

moving a relative location of said substrate to the condensed laser beam along a third direction orthogonal to said first direction while irradiating the non-single crystalline semiconductor layer with the condensed laser beam whereby the non-single crystalline semiconductor layer is crystallized;

removing an insulating layer comprising silicon oxide from an upper surface of the crystallized semiconductor layer; and

forming a plurality of thin film transistors using the crystallized semiconductor layer as at least channel regions of the thin film transistors.

152. A method of manufacturing a plurality of thin film transistors, comprising steps of:

forming an ion blocking film over a substrate;

forming a non-single crystalline semiconductor layer over said ion blocking film, said non-single crystalline semiconductor layer being substantially intrinsic and doped with a dopant selected from the group consisting of boron and arsenic;

providing a first laser beam having a first cross section;

expanding said first cross section of the first pulsed laser beam along a first direction;

condensing the expanded laser beam along a second direction orthogonal to said first direction;

irradiating the non-single crystalline semiconductor layer with the condensed laser beam having a second cross section at a surface of the non-single crystalline semiconductor layer wherein a length of said second cross section along said first direction is longer than that of said first cross section and a width of said second cross section along said second direction is smaller than that of said first cross section;

moving a relative location of said substrate to the condensed laser beam along a third direction orthogonal to said first direction while irradiating the non-single crystalline semiconductor layer with the condensed laser beam whereby the non-single crystalline semiconductor layer is crystallized; and

forming a plurality of thin film transistors using the crystallized semiconductor layer as at least channel regions of the thin film transistors.

153. A method of manufacturing a plurality of thin film transistors comprising:

forming an ion blocking film over a substrate;

forming a plurality of semiconductor islands over the ion blocking film, each of said semiconductor islands comprising crystallized silicon;

forming a gate insulating film on said plurality of semiconductor islands wherein said gate insulating film covers a surface of the ion blocking film, said surface being exposed between the plurality of semiconductor islands;

forming gate electrodes over the semiconductor islands with the gate insulating film interposed therebetween,

wherein the formation of said plurality of semiconductor islands comprises steps of:

providing a first laser beam having a first cross section;

expanding said first cross section of the first pulsed laser beam along a first direction;

condensing the expanded laser beam along a second direction orthogonal to said first direction; and

directing the condensed laser beam to the substrate while moving the substrate along a third direction orthogonal to said first direction,

wherein the condensed laser beam has a second cross section on the substrate wherein a length of said second cross section along said first direction is longer than that of said first cross section and a width of said second cross section along said second direction is smaller than that of said first cross section.

154. A method of manufacturing a plurality of thin film transistors comprising:

forming an ion blocking film over a substrate;

forming a plurality of semiconductor islands over the ion blocking film, each of said semiconductor islands comprising crystallized silicon;

forming a gate insulating film on said plurality of semiconductor islands;

forming metal gate electrodes over the semiconductor islands with the gate insulating film interposed therebetween;

introducing an impurity into portions of the semiconductor islands to form source and drain regions in each of the semiconductor islands with said gate electrodes used as a mask,

wherein the formation of said plurality of semiconductor islands comprises steps of:

providing a first laser beam having a first cross section;

expanding said first cross section of the first pulsed laser beam along a first direction;

condensing the expanded laser beam along a second direction orthogonal to said first direction; and

directing the condensed laser beam to the substrate while moving the substrate along a third direction orthogonal to said first direction,

wherein the condensed laser beam has a second cross section on the substrate wherein a length of said second cross section along said first direction is longer than that of said first cross section and a width of said second cross section along said second direction is smaller than that of said first cross section.

155. The method according to claim 151 or 152 wherein said non-single crystalline semiconductor layer comprises amorphous silicon.

156. The method according to claim 151 or 152 wherein said non-single crystalline semiconductor layer comprises solid phase crystallized silicon.

157. The method according to claim 152 further comprising a step of removing an insulating layer comprising silicon oxide from an upper surface of the crystallized semiconductor layer.

158. The method according to any one of claim 151 to 154 wherein said ion blocking film comprises silicon oxide.

159. The method according to any one of claim 151 to 154 wherein said ion blocking film comprises silicon nitride.

160. The method according to any one of claim 151 to 154 wherein said ion blocking film comprises non-doped silicon oxide.

161. The method according to any one of claim 151 to 154 further comprising a step of removing a peripheral portion of the expanded laser beam through a mask before the step of condensing the expanded laser beam wherein said peripheral portion includes at least edges of the expanded laser beam extending along said first direction.

162. The method according to any one of claim 151 to 154 wherein said substrate is moved.

163. The method according to any one of claim 151 to 154 wherein said ion blocking film blocks sodium from the substrate.

164. A method of manufacturing an active matrix display device having an active matrix circuit and a peripheral circuit for driving pixel TFTs, said method comprising:

forming an ion blocking film over a substrate;

forming a plurality of semiconductor islands for said active matrix circuit and said peripheral circuit over the ion blocking film, each of said semiconductor islands comprising crystallized silicon;

forming a gate insulating film on said plurality of semiconductor islands wherein said gate insulating film covers a surface of the ion blocking film, said surface being exposed between the plurality of semiconductor islands;

forming gate electrodes over the semiconductor islands with the gate insulating film interposed therebetween,

wherein the formation of said plurality of semiconductor islands comprises steps of:

providing a first laser beam having a first cross section;

expanding said first cross section of the first pulsed laser beam along a first direction;

condensing the expanded laser beam along a second direction orthogonal to said first direction; and

directing the condensed laser beam to the substrate while moving the substrate along a third direction orthogonal to said first direction,

wherein the condensed laser beam has a second cross section on the substrate wherein a length of said second cross section along said first direction is longer than that of said first cross section and a width of said second cross section along said second direction is smaller than that of said first cross section.

165. A method of manufacturing an active matrix display device having an active matrix circuit and a peripheral circuit, said method comprising:

forming an ion blocking film over a substrate;

forming a plurality of semiconductor islands for said active matrix circuit and said peripheral circuit over the ion blocking film, each of said semiconductor islands comprising crystallized silicon;

forming a gate insulating film on said plurality of semiconductor islands;

forming metal gate electrodes over the semiconductor islands with the gate insulating film interposed therebetween;

introducing an impurity into portions of the semiconductor islands to form source and drain regions in each of the semiconductor islands with said gate electrodes used as a mask,

wherein the formation of said plurality of semiconductor islands comprises steps of:

providing a first laser beam having a first cross section;

expanding said first cross section of the first pulsed laser beam along a first direction;

condensing the expanded laser beam along a second direction orthogonal to said first direction; and

directing the condensed laser beam to the substrate while moving a relative location of the substrate to the condensed laser beam along a third direction orthogonal to said first direction,

wherein the condensed laser beam has a second cross section on the substrate wherein a length of said second cross section along said first direction is longer than that of said first cross section and a width of said second cross section along said second direction is smaller than that of said first cross section.

166. The method according to claim 71 or 76, wherein said non-single crystalline semiconductor layer comprises amorphous silicon.

167. The method according to claim 71 or 76, wherein said non-single crystalline semiconductor layer comprises solid phase crystallized silicon.

168. The method according to claim 76, further comprising a step of removing an insulating layer comprising silicon oxide from an upper surface of the crystallized semiconductor layer.

169. The method according to any one of claims 164-165, wherein said ion blocking film comprises silicon oxide.

170. The method according to any one of claims 164-165, wherein said ion blocking film comprises silicon nitride.

171. The method according to any one of claims 164-165, wherein said ion blocking film comprises non-doped silicon oxide.

172. The method according to any one of claims 164-165, further comprising a step of removing a peripheral portion of the expanded laser beam through a mask before the step of condensing the expanded laser beam wherein said peripheral portion includes at least edges of the expanded laser beam extending along said first direction.

173. The method according to any one of claims 71, 76 and 164-165 wherein said substrate is moved.

174. The method according to any one of claims 71, 76 and 164-165 wherein said ion blocking film blocks sodium from the substrate.

175. The method according to anyone of claims 61, 66, 71, 76, 140, 141, 151, 152, 164 and 165 wherein said substrate is a glass substrate.

176. The method according to claim 61, wherein said insulating layer comprising silicon oxide is formed before the irradiating with the condensed laser beam.

177. The method according to claim 71, wherein said insulating layer comprising silicon oxide is formed before the irradiating with the condensed laser beam.

178. The method according to claim 144, wherein said insulating layer comprising silicon oxide is formed before the irradiating with the condensed laser beam.

179. The method according to claim 151, wherein said insulating layer comprising silicon oxide is formed before the irradiating with the condensed laser beam.

180. The method according to claim 168, wherein said insulating layer comprising silicon oxide is formed before the irradiating with the condensed laser beam.

X. EVIDENCE APPENDIX

U.S. Patent No. 7,416,907 B2 issued August 26, 2008 to Yamazaki et al.

U.S. Patent No. 7,381,599 B2 issued June 3, 2008 to Konuma et al.

XI. RELATED PROCEEDINGS APPENDIX

There are no related proceedings to this Appeal.